Remarks:

Reconsideration of the application is requested.

Claims 1-2 remain in the application. Claim 2 has been amended. Claim 1 has been withdrawn from consideration.

In item 4 on pages 2-3 of the above-identified Office action, the drawings have been objected to under 37 CFR 1.83(a) as not showing every feature of the invention specified in the claims.

More specifically, the Examiner has stated that the matrix of contact holes down to the semiconductor substrate in the insulating layer in accordance with respective semiconductor elements; each of the implantations (first and second) and the corresponding masks used for the implants; the undoped surface of the substrate which left in the third group of contact holes; the contact plugs; and the further provided contact region outside the bit definition region must be shown or the feature(s) cancelled from the claim(s).

FIG 1 and FIG 2 have been amended to show the above-mentioned features: multiple contact holes 25, multiple contact plugs 40, masks 32, a first implantation I_1 and a second implantation I_2, and a further contact region 40' outside the bit definition region. Now all three types of bit definition regions (doped

with a first conductivity type, doped with a second conductivity type and undoped) are shown. The specification has also been amended accordingly.

In item 5 on page 3 of the above-identified Office action, the drawings have been objected to under 37 CFR 1.83(a) as failing to show the above-mentioned features as described in the specification. The drawings have been amended as discussed above.

In item 6 on page 3 of the above-identified Office action, the drawings have been objected to under 37 CFR 1.83(b) as being incomplete. The drawings have been amended as discussed above.

In deference to the requirement in item 7 on page 3 of the above-identified Office action, the abstract of the disclosure has been amended and the Examiner's suggested correction has been made.

In item 10 on page 4 of the above-identified Office action, claim 2 has been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner has stated that the step "leaving the surface region..." in claim 2 is indefinite and

unclear in that it does not accurately describe that this region is left undoped, as explained in the specification.

Claim 2 has been amended by adding the word "undoped" at the end of the paragraph describing this step.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, second paragraph. Should the Examiner find any further objectionable items, counsel would appreciate a telephone call during which the matter may be resolved. The above-noted changes to the claims are provided solely for cosmetic and/or clarificatory reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claims for any reason related to the statutory requirements for a patent.

In item 12 on page 5 of the above-mentioned Office action, claim 2 has been rejected as being anticipated by Sato (US Pat. No. 5,960,283) under 35 U.S.C. § 102(b). In item 13 on page 5 of the above-mentioned Office action, claim 2 has been rejected as being anticipated by Hikawa et al. (US Pat. No. 5,753,553) under 35 U.S.C. § 102(b).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and

the claims have, therefore, not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> performing a first implantation with a dopant of the first conductivity type into a first group of the contact holes with remaining ones of the contact holes being masked;
>
> performing a second implantation with a dopant of a second conductivity type into a second group of the contact holes with remaining ones of the contact holes being masked; and
>
> leaving the surface region of the semiconductor substrate situated underneath the respective contact holes in a substrate doping in a third group of contact holes undoped.

The invention of the instant application provides a method for fabricating a semiconductor memory device having three-value logic per memory element by using only two implantations, thus makes it possible to fabricate a cost-effective multilevel ROM. This feature is not shown or suggested by Sato or Hiwaka et al.

According to the invention of the instant application, in contrast to Sato or Hiwaka et al., the memory cells are defined by resistors having different resistance values. The

different resistance values can be assessed during read-out by a suitable evaluation circuit.

Clearly, none of the references shows "performing a first implantation with a dopant of the first conductivity type into a first group of the contact holes with remaining ones of the contact holes being masked; performing a second implantation with a dopant of a second conductivity type into a second group of the contact holes with remaining ones of the contact holes being masked; and leaving the surface region of the semiconductor substrate situated underneath the respective contact holes in a substrate doping in a third group of contact holes undoped", as recited in claim 2 of the instant application.

Claim 2 is, therefore, believed to be patentable over the art.

In view of the foregoing, reconsideration and allowance of claim 2 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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Marked-Up Version of the Amended Paragraphs in the Specification and Marked-Up Version of the Amended Claims:

The abstract of the disclosure now reads:

Abstract of the Disclosure:

A method for fabricating a semiconductor memory device is described [that is formed of a semiconductor substrate]. An insulating layer is disposed on [the] a semiconductor substrate. A matrix of semiconductor memory elements is disposed in the substrate. The semiconductor memory elements include a plurality of contact holes formed in the insulating layer. One contact hole is formed in the insulating layer for each of the semiconductor memory elements. A bit definition region is disposed in the semiconductor substrate underneath each of the contact holes. A contact plug is disposed in each of the contact holes and is in electrical contact with the bit definition region. The bit definition region is configured such that a contact resistance between the semiconductor substrate and the contact plug defines a bit to be stored in the semiconductor memory elements. An evaluation circuit is connected to and evaluates the contact resistance of the semiconductor memory elements.

The paragraph starting on page 11, line 3 and ending on page 11, line 10 now reads as:

In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown a semiconductor memory device 1 formed of a substrate 10, an insulating layer 20 disposed on the substrate 10, [a] contact [hole] holes 25 formed in the insulating layer 20, [a] bit definition [region] regions 30, and an implantation [I] I_1 and an implantation I_2.

The paragraph starting on page 12, line 14 and ending on page 12, line 17 now reads as:

All the contact holes 25 are defined and etched free photolithographically. The first implantation [I] I_1 into a first group of the contact holes 25 is then performed using a dopant of the first conductivity type n.

The paragraph starting on page 12, line 19 and ending on page 12, line 21 now reads as:

A second implantation I_2 is then performed using a dopant of a second conductivity type p in a second group of the contact holes 25.

The paragraph starting on page 13, line 1 and ending on

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page 13, line 3 now reads as:

A third group of the contact holes 25 remains covered by masks 32 during both implantations, that is to say does not receive implantation.

The paragraph starting on page 13, line 5 and ending on page 13, line 9 now reads as:

There are, then, the following semiconductor memory cells with increasing contact resistance: a contact implantation like the underlying substrate (e.g. like diffusion implantation), no implantation and contact implantation opposite to the underlying substrate[, Fig. 1 showing only the first case].

The paragraph starting on page 13, line 20 and ending on page 13, line 21 now reads as:

In Fig. 2, in addition to the reference symbols already introduced, [a] contact [plug] plugs 40 [is] are provided.

The paragraph starting on page 14, line 4 and ending on page 14, line 9 now reads as:

The substrate 10 expediently has a strip-type conductor strip structure, e.g. polysilicon or diffusion strips, the strips

each forming a second terminal of the memory cells on a top side of the substrate, which, in addition to the respective contact plug 40, forms a terminal 40' for an evaluation circuit with a resistance measuring device.

Claim 2(amended). A method for fabricating a semiconductor memory device, which comprises the steps of:

providing a semiconductor substrate having a first conductivity type;

providing an insulating layer on the semiconductor substrate;

forming a matrix of contact holes down to the semiconductor substrate in the insulating layer in accordance with respective the semiconductor memory elements;

providing a surface region of the semiconductor substrate situated underneath each of the contact holes with a contact resistance in accordance with a bit to be stored in a respective semiconductor memory element as a bit definition region of the respective semiconductor memory element, the contact resistance formed by the steps of:

performing a first implantation with a dopant of the first conductivity type into a first group of the contact

holes with remaining ones of the contact holes being masked;

performing a second implantation with a dopant of a second conductivity type into a second group of the contact holes with remaining ones of the contact holes being masked; and

leaving the surface region of the semiconductor substrate situated underneath the respective contact holes in a substrate doping in a third group of contact holes undoped;

providing contact plugs in the contact holes, the contact plugs being in electrical contact with the bit definition region; and

providing a further contact region located in the semiconductor substrate outside the bit definition region.